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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
GUILL, RUSSELL L	

ART UNIT	PAPER NUMBER
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/060,750	DEVINS ET AL.	
	Examiner	Art Unit	
	Russ Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2 and 8-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2 and 8-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is in response to an Amendment filed October 17, 2008. Claims 28 - 34 were canceled. No claims were added. Claims 2, 8 - 27 are pending. Claims 2, 8 - 27 have been examined. Claims 2, 8 - 27 have been rejected.

Response to Remarks

2. Regarding claims 2 and 8 - 34 rejected under 35 USC § 112, second paragraph:

a. Applicant's arguments have been fully considered, and are not persuasive.

b. The Applicant argues:

c. [0002] The Office Action states, "The specification appears to be directed to a software invention that is implemented in a computer. Especially see the specification paragraphs [0004][0005] that appear to define an SOC as cores, and a core is embodied as a simulatable HDL model, and may be in the form of a netlist. Currently, the elements of the claim appear to have an interpretation as either physical hardware or a software model *(see especially paragraph [00251, and paragraphs [00011-1'00081).* (Office Action, page 3, section ii).

d. [0003] Paragraph [0003] of the Background section of the Specification recites in relevant part, "Hardware verification typically entails the use of software "models" of design logic." Paragraph [0004] of the Background section of the Specification recites in relevant part, "The term 'SOC' [i.e., system-on-a-chip] *as* used herein refers to combinations of discrete logic blocks, often referred to as 'cores', each performing a different function of group of functions. A SOC integrates a plurality of cores into a single silicon device, thereby providing a wide range of functions in a highly compact form." Paragraph [0005] of the Background section of the Specification recites in relevant part, "In its developmental stage, a core is typically embodied as a simulatable HDL model

.... A core may be in the form of a netlist ." Paragraph [0006] of the Background section of the Specification recites in relevant part, "Verification of a SOC presents challenges because of the number of cores and the complexity of interactions involved, both between the cores internally to the SOC, and between the SOC and external logic." Paragraph [0007] of the Background section of the Specification recites in relevant part, "According to one standard technique, already-verified models are used to test other models. The electronic design automation (EDA) industry has reached a level of sophistication wherein vendors offer standardized models for use in verification of other models still in development." Paragraph [0008] of the Background section of the Specification recites in relevant part, "However, there are disadvantages associated with using standardized models."

e. [0004] Applicants now recite the first paragraph, i.e., [0010], of the Summary of the Invention section, "In view of the foregoing and other problems, disadvantages, and drawbacks of conventional verification test benches, the present invention has been devised, and it is an object of the present invention to provide a structure that attaches an external model to a SOC interface and to an external bus interface unit."

f. [0005] Applicants respectfully submit that paragraphs [0002]-[0009] describe the related art, which may be paraphrased as follows: Hardware verification of integrated circuits typically entails use of software models for logic blocks. A system-on-a chip (SOC) comprises a number of logic blocks, also called "cores", which are integrated into a single silicon device. Conventional techniques of verification of the logic blocks of an SOC may use HDL models or netlists. However, hardware verification of an SOC presents challenges because of the complexity of interaction between logic blocks of the SOC and between the SOC and external logic devices. Standardized software models used for models of the

gic blocks, still in development, have disadvantages.

g. [0006] In other words, according to the related art section of the Specification, hardware verification by software models of the logic blocks, comprising an SOC, have disadvantages.

h. [0007] Therefore, as recited in paragraph [0010] of the Summary of the Invention, another approach to overcoming the disadvantages of conventional software modeling of logic blocks for hardware verification of an SOC are described, i.e., a structure (i.e., hardware) that attaches an external model (i.e., hardware) to a SOC interface (i.e., hardware) and to an external bus interface unit (i.e., hardware)."

i. The Examiner respectfully replies:

ii. While the Examiner appreciates the Applicant's argument, the Examiner respectfully disagrees, as follows.

iii. The argument recites above, "A system-on-a chip (SOC) comprises a number of logic blocks, also called "cores", which are integrated into a single silicon device". While an SOC *may* be a silicon device, the specification appears to be directed to a software SOC. As discussed in paragraphs [0001] – [0008] of the specification, an SOC may be interpreted as software. Also, see paragraph [0025] which recites, "Figure 2 shows a computer system which can be used to implement the present invention", which appears to imply that the invention is not a hardware SOC, since the invention is implemented on a computer with a simulator. Since the preceding arguments are also used below for the rejections under 35 U.S.C. § 101, the Examiner remarks that if a claim has both statutory and non-statutory interpretations, the claim must be amended to have only a statutory interpretation. If the SOC is hardware,

then the claims should be amended to indicate this. If the SOC is software, then the claims should be amended to include hardware.

iv. The last paragraph of the argument above recites, ", i.e., a structure (i.e., hardware) that attaches an external model (i.e., hardware) to a SOC interface (i.e., hardware) and to an external bus interface unit (i.e., hardware)". The Examiner respectfully disagrees with the interpretation, as follows.

(1) The recited structure ("a structure (i.e., hardware)"), appears to be a software structure (*see specification paragraph [0019], "an SOC structure 300 (e.g., a verification test bench)", where the verification test bench is software as shown at least in figure 2, element 450; and see specification, paragraph [0025], "Programming structures and functionality are implemented in computer-executable instructions as disclosed herein-above for performing steps of the method . . . ". Also, "Figure 2 shows a computer system which can be used to implement the present invention", which appears to imply that the invention is not a hardware SOC*).

(2) The recited external model ("an external model (i.e., hardware)"), appears to be a software external model because the external model appears to be the verification test bench, which is software as shown in figure 2, element 450.

(3) The recited SOC interface ("SOC interface (i.e., hardware)"), appears to be software because as recited in the specification, "The term "SOC" as used herein refers to combinations of discrete logic blocks, often referred to as "cores"" (*paragraph [0004]*), and "A core may be in the form of a netlist" (*paragraph [0005]*), and "In its

developmental stages, a core is typically embodied as a simulatable HDL model written at some level of abstraction" (*paragraph [0005]*).

(4) The recited external bus interface ("external bus interface unit (i.e., hardware)"), appears to be software because it is part of the verification test bench, which is software as shown in figure 2, element 450.

i. The Applicant argues:

j. [0008] As is known to those in the art of chip design and verification, verification by software has its disadvantages. In particular, race conditions are difficult to resolve through software verification. For example, imagine a 2-input NAND gate within a chip to be verified. The first input to the NAND gate derives from a logic block comprising 15 gates, whereas the second input to the NAND gate derives from a logic block comprising but 10 gates. The first input signal will arrive at the NAND before the second input (assuming length and impedances of the input lines are approximately equal). That is, the proper output for the NAND gate is not when the first input arrives but is delayed by the timing of the second input, and whatever delays there are associated with the NAND gate itself. In the floor planning of an SOC, unanticipated delays between logic blocks (even when CLOCKed) can lead to errors from expected functional outputs. Thus, the present invention uses a hardware SOC to test itself, by running test patterns on itself, sending the results to an external verification test bench including a verification interface model, which also receives signals from the SOC interface, to verify the hardware logic of the hardware SOC.

i. The Examiner respectfully replies:

ii. The Applicant asserts above that the SOC is hardware, but as discussed above, the SOC at least has an interpretation as software.

Further, the invention appears to be directed entirely to a software SOC; please see paragraph [0025] which recites, "Figure 2 shows a computer system which can be used to implement the present invention", which appears to imply that the invention is not a hardware SOC, since the invention is implemented on a computer with a simulator.

iii. Further, it was common knowledge in the art to extract timing from floor plans and back annotate the HDL to account for timing in the HDL simulation.

k. The Applicant argues:

l. [0009] The Office Action especially refers to paragraph [0025] of the Specification, which refers to Fig. 2, of the application; however, all of the pending claims, are clearly shown in Fig. 1 of the application.

i. The Examiner respectfully replies:

ii. The entire specification is considered to apply to the claims, at least because paragraph [0025] recites, "Figure 2 shows a computer system which can be used to implement the present invention", which appears to include figure 1. Further, the interpretation of an SOC in figure 1 is influenced by the recited, "The term "SOC" as used herein refers to combinations of discrete logic blocks, often referred to as "cores"" (*paragraph [0004]*), and "A core may be in the form of a netlist" (*paragraph [0005]*), and "In its developmental stages, a core is typically embodied as a simulatable HDL model written at some level of abstraction" (*paragraph [0005]*).

m. The Applicant argues:

n. [0010] The Office Action also states, "The specification appears to be directed to verification of HDL models of a SOC *(see especially paragraphs 10001]-10008D,* and does not appear to intend to support a system with a physical CPU, a physical SOC interface, and physical EBIU interfaces. Especially see the specification paragraphs [0004]-[0005] that appear to define an SOC as cores, and a core is embodied as a simulatable HDL model, and may be in the form of a netlist." (Office Action, page 3, section iii).

o. [0011] For the identical reasons outlined above, with respect to the Office Action's assertion that the specification appears to be directed to a software invention that is implemented in a computer, Applicants respectfully argue that paragraphs [0002]-[0008] describe the convention related art and not the present invention.

i. The Examiner respectfully replies:

ii. Paragraph [0004] recites, "The term "SOC" as used *herein*". The term "herein" appears to refer to the entire specification. Thus, paragraph [0004] and its related support in the other paragraphs appear to refer to the invention.

p. The Applicant argues:

q. [0012] The present invention is clearly described in paragraphs [0019]-[0024] and [0026], the elements of which are shown in Fig. 1 of the specification. As a convenience to the Examiner, Applicants provide the following annotated independent claims, in which the annotations refer to the present invention's features in the text, indicated by paragraph number and line numbers within each paragraph, and the figures, indicated by Figure number and element number, of the Specification.

r. [0013] For at least the reasons outlined above, Applicants respectfully submit that currently amended, independent claims 2, 8, 15, and 21, and dependent claims 9-14, 16-20, and 22-27, particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Therefore, Applicants further respectfully submit that currently amended claims 2 and 8-27 fulfill the statutory requirements of 35 U.S.C. § 112, second paragraph. The rejection of canceled claims 28-34 is moot. Withdrawal of the rejection of claims 2 and 8-34 under U.S.C. § 112, second paragraph, is respectfully solicited.

i. The Examiner respectfully replies:

ii. The rejections are maintained as discussed above.

3. Regarding claims 2 and 8 - 34 rejected under 35 USC § 101:

a. Applicant's arguments have been fully considered, and are partly persuasive, and partly not persuasive, as discussed below.

b. The Applicant argues:

c. [0014]Claims 2, and 8-34 stand rejected under 35 U.S.C. § 101 because the Office Action asserts that the claimed invention is directed to non-statutory subject matter.

d. [0015]The Office Action states, "The specification appears to be directed to a software invention that is implemented in a computer. Especially see the specification paragraphs [0004]-[0005] that appear to define an SOC as cores, and a core is embodied as a simulatable HDL model, and may be in the form of a netlist. Currently, the elements of the claim appear to have an interpretation as either physical hardware or a software model." (Office Action, page 5, section ii).

e. [0016] Applicants respectfully submit that the 35 U.S.C. § 101 rejection of the

claims, immediately above, is based on the identical assertion for the 35 U.S.C. 112, second paragraph, rejection on page 3, section ii of the Office Action. Therefore, Applicants' arguments are also identical to those presented above, with respect to the rejection of the claims under 35 U.S.C. §112, second paragraph.

i. The Examiner respectfully replies:

ii. Since Applicant's arguments are the same as the arguments regarding 35 USC § 112, second paragraph, the Examiner's reply is the same. Accordingly, the rejections are maintained.

f. The Applicant argues:

g. [0017] The Office Action also states, "The act of verification does not appear to produce a tangible result. The act of verification does not appear to produce an output that could be a tangible result." (Office Action, page 6, section ii).

h. [0018]Applicants have currently amended, independent claims 2, 15, and 21 to include the limitation, "wherein said verification case checks for correctness of said outputted data from said verification interface model to said SOC interface by said second set of signals and records a verification case status", and independent claim 8 to include the similar limitation, "wherein said verification case checks for correctness of said outputted data from said verification interface model to said SOC interface by said second set of signals via said first internal bus and records a verification case status". These limitations are supported at paragraph [0023], the last 2 lines).

i. [0019] Applicants respectfully submit that recording a verification case status, as described by the currently amended claims, produces a tangible result, i.e., the record of the verification case status.

i. The Examiner respectfully replies:

ii. Applicant's arguments are persuasive. Further, the Examiner thanks the Applicant for providing the location of support in the specification, which was useful to expedite the examination process.

j. The Applicant argues:

k. [0020] For at least the reasons outlined above, Applicants respectfully submit that the currently amended claims fulfill the statutory requirements of 35 U.S.C. § 101. The rejection of canceled claims 28-34 is moot. Withdrawal of the rejection of claims 2 and 8-34 under 35 U.S.C. §101 is respectfully solicited.

i. The Examiner respectfully replies:

ii. The rejections are maintained for the reasons discussed above.

4. Regarding claims 2 and 8 - 34 rejected under 35 USC § 112, first paragraph:

a. Applicant's arguments have been fully considered, and are not persuasive, as discussed below.

b. The Applicant argues:

c. [0021]Claims 2 and 8-34 stand rejected under 35 U.S.C. §112, first paragraph.

d. [0022] The Office Action states, "Regarding claim 2 and dependent claims: claim 2 recites a CPU, an SOC interface and EBIU interfaces that the Applicant has argued as being physical hardware. The specification appears to be directed to software models of a CPU, an SOC interface and EBIU interfaces that are implemented in a computer system *(see especially paragraph [0025], and paragraphs [0001]-[0008]).* (Office Action, page 7, section 13.a). The Office

Action continues to make substantially similar statements regarding the other independent claims and their dependent claims. (Office Action, page 8.b to page 9).

e. [0023] The Office Action, in its rejection of the claims under 35 U.S.C. 112, second paragraph, stated, "The specification appears to be directed to a software invention that is implemented in a computer. Especially see the specification paragraphs [0004]-[0005] that appear to define an SOC as cores, and a core is embodied as a simulatable HDL model, and may be in the form of a netlist. Currently, the elements of the claim appear to have an interpretation as either physical hardware or a software model *(see especially paragraph [0025], and paragraphs [00011-10008]).* (Office Action, page 3, section ii).

f. [0024] Applicants respectfully submit that the 35 U.S.C. § 112, first paragraph, rejection of the claims, immediately above, is based on the substantially similar assertion for the 35 U.S.C. 112, second paragraph, rejection on page 3, section ii of the Office Action. Therefore, Applicants' arguments are identical to those presented above, with respect to the rejection of the claims under 35 U.S.C. § 112, second paragraph.

g. [0025] For at least the reasons outlined above, Applicants respectfully submit that the currently amended claims comply with the written description requirement and thus, fulfill the statutory requirements of 35 U.S.C. §112, first paragraph. The rejection of canceled claims 2834 is moot. Withdrawal of the rejection of claims 2 and 8-34 under 35 U.S.C. §112, first paragraph, is respectfully solicited.

i. The Examiner respectfully replies:

ii. Since Applicant's arguments are the same as the arguments regarding 35 USC § 112, second paragraph, the Examiner's reply is the same. Accordingly, the rejections are maintained.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 2 and 8 - 27 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

a. Regarding claim 2 and dependent claims: claim 2 recites a CPU, an SOC interface and EBIU interfaces that the Applicant has argued as being physical hardware; however, the specification appears to be directed to software models of a CPU, an SOC interface and EBIU interfaces that are implemented in a computer system (*see especially paragraph [0025], "Figure 2 shows a computer system which can be used to implement the present invention", and paragraphs [0001] – [0008]*). The specification appears to be directed to verification of HDL models of a SOC (*see especially paragraphs [0001] – [0008]*), and does not appear to intend to support a system with a physical CPU, a physical SOC interface, and physical EBIU interfaces. Especially see the specification paragraphs [0004] - [0005] that appear to define an SOC as cores, and a core is embodied as a simulatable HDL model, and may be in the form of a netlist.

b. Regarding claim 8 and dependent claims: claim 8 recites a CPU, an SOC interface and EBIU interfaces that the Applicant has argued as being physical hardware. The specification appears to be directed to software models of a CPU, an SOC interface and EBIU interfaces that are implemented in a computer system (*see especially paragraph [0025], "Figure 2 shows a computer system which can be used to implement the present invention", and paragraphs [0001] – [0008]*). The specification appears to be directed to verification of HDL models of a SOC (*see especially paragraphs [0001] – [0008]*), and does not appear to intend to support a system with a physical CPU, a physical SOC interface, and physical EBIU interfaces. Especially see the specification paragraphs [0004] - [0005] that appear to define an SOC as cores, and a core is embodied as a simulatable HDL model, and may be in the form of a netlist.

c. Regarding claim 15 and dependent claims: claim 15 recites a CPU, an SOC interface and EBIU interfaces that the Applicant has argued as being physical hardware. The specification appears to be directed to software models of a CPU, an SOC interface and EBIU interfaces that are implemented in a computer system (*see especially paragraph [0025], "Figure 2 shows a computer system which can be used to implement the present invention", and paragraphs [0001] – [0008]*). The specification appears to be directed to verification of HDL models of a SOC (*see especially paragraphs [0001] – [0008]*), and does not appear to intend to support a system with a physical CPU, a physical SOC interface, and physical EBIU interfaces. Especially see the specification paragraphs [0004] - [0005] that appear to define an SOC as cores, and a core is embodied as a simulatable HDL model, and may be in the form of a netlist.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

a. Claims 2, 8 – 27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

i. Regarding independent claims 2, 8 and 15, and dependent claims: the independent claims 2, 8 and 15 appear to be directed to a physical hardware system, however the specification appears to be directed to a software model of a physical hardware system (*Especially see the specification paragraphs [0004] - [0005] that appear to define an SOC as cores, and a core is embodied as a simulatable HDL model, and may be in the form of a netlist*). It is unclear whether the claims are directed to physical hardware or a software model. Any elements of the claims that are intended to be physical hardware should be clearly distinguished as physical hardware, and similarly, software elements should be distinguished.

ii. Regarding independent claims 21, and dependent claims: the independent claims appear to be directed to a method that uses physical hardware; however the specification appears to be directed to a software model of a physical hardware system (*Especially see the specification paragraphs [0004] - [0005] that appear to define an SOC as cores, and a core is embodied as a simulatable HDL model, and may be in the form of a netlist*). It is unclear whether the claims are directed to a method that uses physical hardware or a software model. Any elements of the claims that are intended to be physical hardware should be clearly distinguished as

physical hardware, and similarly, software elements should be distinguished.

Claim Rejections - 35 USC § 101

8. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

9. Regarding claims 21 – 27, the method is performed in a software environment inherently requiring a computer to perform the method, and thus is considered statutory because it is inherently tied to a computer to perform the method.

10. Claims 2, 8 – 14 and 15 – 20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

a. Regarding claims 2, 8 – 14, 15 - 20, the claims are directed to a system for verification of integrated circuit logic of a system-on-chip, but none of the claim limitations appear to expressly or inherently require tangible physical components (*Especially see the specification paragraphs [0004] - [0005] that appear to define an SOC as cores, and a core is embodied as a simulatable HDL model, and may be in the form of a netlist. Also especially paragraph [0025], "Figure 2 shows a computer system which can be used to implement the present invention", and paragraphs [0001] – [0008]*). An ordinary artisan interpreting the claim in light of the specification would reasonably interpret the claim as encompassing a purely software system. All of the components recited in the claim appear to have a reasonable interpretation as software elements, as discussed above, including the CPU, the SOC interface, and the EBIU interfaces. A claim that has both statutory and non-

statutory interpretations must be amended to have only statutory interpretations. Any elements of the claim that are intended to be physical hardware should be clearly distinguished as physical hardware.

Allowable Subject Matter

11. Any indication of allowability is withheld pending resolution of the outstanding rejections.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

13. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

14. The prior art made of record in a previous Office action, and not relied upon, is considered pertinent to the applicant's disclosure, and teaches common knowledge in the art:

a. Robert Devins, "SOC Verification Software - Test Operating System", April 2001, retrieved from the internet at http://www.eda-stds.org/edps/edp01/PAPERS/devins.pdf, pages 185 – 190; teaches SOC verification wherein the SOC controls the testbench through a parallel channel.

b. M. Morris Mano, "Computer System Architecture", second edition, 1982, Prentice-Hall, pages 272, 433; appears to teach the essential architecture of the invention in figure 7-20.

c. Tom Shanley and Don Anderson, "ISA System Architecture", third edition, 1995, Addison-Wesley, pages 13, 16 – 19, 54, 125, 154, 241; teaches separate buses for address, data and control signals, and external bus interface units (figure 5-1).

d. Auerbach (U.S. Patent Number 6,199,126) teaches an EBIU on both ends of a bus (*figure 7*).

e. Nightingale (U.S. Patent Application Publication 2002/0183956) teaches SOC test software in an SOC controlling an external device.

f. Bergamaschi et al., "Designing systems-on-chip using cores", June 5, 2000, Proceedings of the 37th Design Automation Conference 2000, pages 420 – 425; teaches a slave device with a separate high-speed data bus and low-speed control bus connected to a SOC processor core (*figure 1, PLB Slaves, DCR bus, PLB Masters (e.g. CPU)*).

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russ Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday – Friday 9:30 AM – 6:00 PM.

16. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.

17. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Russ Guill
Examiner
Art Unit 2123

RG

/Paul L Rodriguez/

Supervisory Patent Examiner,
Art Unit 2123